Remarks

Support for claim 14 as amended in the Specification as filed

FIGs. 2 and 3 of the Specification as filed and the discussion of those Figures beginning at page 10, line 6 of the Specification as filed show clearly that the integrated circuit claimed in claim 14 is "constructed on one chip". That "each data stream processor process[es] a stream of data from the data stream input and/or output the data stream processor is coupled to as the data stream is received from the data stream input and/or transmitted to the data stream output" is apparent from the section *Example of cooperation of the components of DCP 203*, beginning at page 17, line 1 of the Specification as filed.

Patentability of claim 14 as amended

The amendment to claim 14 expressly sets forth two limitations:

- that the integrated circuit is "constructed on one chip"
- that "each data stream processor processes a stream of data ... as the data stream is received from the data stream input and/or transmitted to the data stream output"

Hansen discloses neither of these limitations, and consequently the amendment has overcome the rejection of claim 14 as anticipated by Hansen.

Construction on one chip

The component of Hansen's media processor that processes data streams is processor 100 (FIG. 2); FIG. 19 shows the four-chip chip set used to implement a preferred embodiment of the media processor; in FIG. 19, a single processor 100 is implemented on the PROCESSOR chip. There is thus no chip in the chip set of FIG. 19 which has "the plurality of data stream processors" in an "integrated circuit constructed on one chip" required by claim 14. There is a discussion of possible variations at col. 27, lines 16-25 of Hansen, which reads as follows:

> As those skilled in the art will appreciate, many implementations for the general purpose media processor 12 are possible in addition to the four-chip implementation described above. Rather than an integrated approach, the general purpose media processor can be implemented in a discrete manner. Alternatively, the general purpose media processor 12 can be implemented in a single integrated circuit, or in an implementation with fewer than four integrated circuit chips. Other combinations and permutations of these implementations are contemplated.

Clearly, Hansen simply does not contemplate an implementation in which there is more than one data stream processor on a chip. That fact is particularly significant given that the Aug. 16, 1995 priority date of Hansen is less than three years earlier than the May 8, 1998 priority date of the present application.

In Examiner's rebuttal of Applicants' arguments in his final rejection, Examiner refers Applicants to col. 5, lines 5-15 and col. 25, lines 53-60 as showing parallel processing. Col. 5, lines 5-15 speaks of "a system for unified media processing having a plurality of general purpose media processors". Each of the "general purpose media processors" is however a device like that shown in FIGs. 7, and 19, namely, a chip set that implements the device of FIG. 7. Here, too, there is no notion of a device having has "the plurality of data stream processors" in an "integrated circuit constructed on one chip" required by claim 14. The same is the case with regard to col. 25, lines 53-60.

Processing data streams as they are input or output

As is apparent from Applicants' FIG. 3 and the discussion of the operation of the IC of FIG. 3, Applicants' data stream processors are located *between* the data stream inputs and outputs and the buffers 231 in SDRAM 229 that hold the data between the time it is received in IC 203 and transmitted from IC 203. The data stream processors are located in that position because, as set forth in amended claim 1, they "process[] a stream of data ... as the data stream is received from the data stream input and/or transmitted to the data stream output". They process an incoming data stream by locating a payload such as an IP packet in the data being transmitted according to the protocol used in the incoming data stream, using the address information in the IP packet to determine what output queue the IP packet should be placed in, while that determination is taking place, placing the IP packet in a buffer 231 in SDRAM 231, making a descriptor specifying the IP packet's buffer 231, and placing the descriptor in the queue for the data stream processor that is to output the packet. When the descriptor reaches the head of that data stream processor's queue, the data stream processor gets the IP packet from the buffer processes it as required for the protocol being used in the outgoing data stream.

As shown in Hansen's FIGs. 7, 13, and 19, in Hansen, by contrast, the processor 100 is located *behind* the memory. High bandwidth interfaces 124 (col. 18, line 41-col. 21, line 67) connect memory 130, Nyquist sampled I/O 128, and the caches 118 and 120 from which

and to which processor 100 reads and writes data, and memory management unit 122, which handles reads and writes by processor 100 to memory 130. All of these devices read from and write to a single memory space (col. 18, line 62-col. 19, line 9). With regard to processor 108, as set forth at col. 11, line 56 through col. 13, line 53, data is transferred to and from processor 100 by bus 108, which connects processor 100 at least to cache 120 and registers 110 (col. 12, line 67-col. 13, line 2). There is thus no direct connection between processor 100 and I/O unit 128. Instead, I/O unit 128 provides incoming data streams to high bandwidth interfaces 124 and receives outgoing data streams from high bandwidth interfaces 124. Prior to being processed by processor 100, the data streams are stored in memory 130; during processing, they are stored in cache 120. Consequently, processor 100 does not "process[] a stream of data from the data stream input and/or output the data stream processor is coupled to as the data stream is received from the data stream input and/or transmitted to the data stream output", as required by claim 14 as amended.

Patentability of claim 14 over Hansen

Since Hansen neither discloses "the plurality of data stream processors" in an "integrated circuit constructed on one chip" required by amended claim 14 nor "processing a stream of data from the data stream input and/or output the data stream processor is coupled to as the data stream is received from the data stream input and/or transmitted to the data stream output" as required by the amended claim, Hansen does not disclose every limitation of the claim as amended and the amendment overcomes the rejection of claim 14 under 35 U.S.C. 102.

Patentability of the dependent claims

Claims 15-23 are all dependent from claim 14 as amended and are consequently therefore all patentable. These claims are, however, also all patentable for the reasons set forth in Applicants' response of 9/28/04. What follows is rebuttals of Examiner's traversals of Applicants' arguments of 9/28/04.

claim 15

The claim requires that the control data processor be a "general-purpose microprocessor that has an industry-standard architecture". A microprocessor's architecture expresses itself in its instruction set, and the instruction sets of industry standard microprocessors simply do not have instructions like those shown in the table MAJOR OPERATION CODES at col. 13 and

14 for performing shuffle, transposition, and swizzle operations. *Because* processor 100 has such instructions, code for processor 100 may not be developed using tools developed for an industry-standard architecture.

claim 17

The amendment to claim 14 makes it clear that the aggregator is on the same chip as the data stream processors and aggregates data stream processors on the chip; what is disclosed in Kolchinsky is a single configurable virtual processor module VPM that is typically implemented on a board to be plugged into a backplane (col. 8, lines 34-44). What is claimed is not the configuration of a single processor, but rather the *aggregation* of a *plurality* of data stream processors. Because Kolchinsky discloses only one VPM, it can necessarily disclose nothing about aggregating a plurality of data stream processors. The same is the case with Hansen's allocation of varying amounts of the processing power of his single processor 100 to various data streams. Claim 17 is consequently patentable in its own right over the combination of references.

Claim 18

Hansen can indeed be used with a plurality of transmission protocols, but there is simply no disclosure in Hansen concerning Fig. 5's Nyquist sampled I/O element 128 beyond its existence and function. There is thus no disclosure whatever of anything concerning claim 18's "configuration circuitry coupled between the plurality of I/O pins and the data stream processor". Murata similarly discloses nothing whatever about anything like claim 18's configuration circuitry. Consequently, the claim is patentable in its own right over the combination of references.

Claim 19

As set forth above, Hansen does not disclose the "data stream processor" of amended claim 14, and consequently does not disclose the control data processor. That being the case, the combination of Hansen with Deb does not disclose the combination of a "control data processor" with a "receive processor" and a "transmit processor" that is required by the claim. That this is so can be seen by comparing FIG. 8 of Dev with Applicants' FIG. 4, which shows that RxSDP 421and TxSDP 427 are both controlled by CP RISC CORE 401. FIG. 4 is described beginning at page 19, line 23 of Applicants' Specification. Because the

combination of Deb with Hansen does not disclose he combination of a "control data processor" with a "receive processor" and a "transmit processor", claims 19-21 are patentable in their own rights over Hansen and Deb. Claims 20 and 21 are further patentable in their own rights for the reasons set forth in Applicants' response of 9/28/04.

Claim 22

The added limitation in claim 22 is

> a context processor that responds to information received from a given data stream processor that is processing a data stream to produce information about *the given data stream's context* and provide the context information to the given data stream processor (emphasis added)

What is abundantly clear from the claim language and the discussion beginning at page 59, line 20 of Applicants' Specification is that the context dealt with by the context processor of claim 22 is the context *of a data stream*; what Yajima discloses is using the context of a pixel *within the data stream* to process the pixel. The distinction is important here because a pixel's context is necessarily much more local and much less complex than a data stream's context, and as would be expected, generating the context of a pixel as disclosed in Yajima is quite different from the data stream context operations such as address translation, CRC computation, and maintenance of traffic statistics that are performed by Applicants' context processor. Since Yajima does not disclose "processing a data stream to produce information about *the given data stream's* context, the claim is patentable in its own right over the reference.

Claim 23

The location in Deb cited by Examiner in his rebuttal sets forth the following:

> In one embodiment, the data structure information may be provided to the host in the form of a "status/descriptor" that is then processed by the host packet processing software. (Deb, col. 11, lines 39-42)

This only states how the host sees the information about the packet; it in no way indicates that the data structure information is stored anywhere but with the packet. That being the case, the cited location has no effect on Applicants' arguments in the response of 9/28/04 as to why claim 23 is patentable in its own right over the cited references.

Conclusion

In this Submission, Applicants have amended claim 14 to better distinguish it from Hansen, have shown that the claim as amended is fully supported by the Specification as filed, have demonstrated that amended claim 14 is patentable over Hansen, and have demonstrated that dependent claims 15 and 17-23 are patentable not only as dependent claims, but also in their own rights over the references. A check for the required RCE fee of $790.00 accompanies this Submission. Applicants respectfully request that Examiner withdraw the finality of his rejection of 6/6/05 as provided by 37 C.F.R. 1. 114 and continue with his examination. Please charge any additional fees required for the RCE or refund any overpayments to deposit account number 501315.

Respectfully submitted,

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